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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	TESSERA 3.0-113 CONT
First Inventor or Application Identifier	Belgacem Haba
Title	METHOD FOR FORMING A MULTI-LAYER CIRCUIT ASSEMBLY
Express Mail Label No.	EL458513424US

JC714 U.S. PTO 09/602091 06/23/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Box Patent Application Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 22] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 3]
4. Oath or Declaration [*Total Pages* 2]
   - a. [ ] Newly executed (original or copy)
   - b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations (1)
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment*

[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08 / 987,521

Prior application information: *Examiner* Dexter Tugbang *Group / Art Unit:* 3729

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Name (Print/Type)	Michael J. Wallace, Jr.	*Registration No. (Attorney/Agent)*	44,486
Signature	Michael J. Wallace, Jr.	*Date*	June 23, 2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Belgacem Haba	
Continuation of Serial No. 08/987,521 filed December 9, 1997	Group Art Unit: 3729
Filed: Herewith	Examiner: Dexter Tugbang
For: METHOD FOR FORMING A MULTI-LAYER CIRCUIT ASSEMBLY	Date: June 23, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

After according a filing date to the above-identified Rule 53(b) Continuation Application, please amend the application as follows:

In the Specification:

At page 1, line 1, please delete "This application".

At page 1, line 1, before "claims benefit of" insert --The present application is a continuation of United States Patent Application 08/987,521 filed December 9, 1997, which--.

In the Claims:

Amend claim 28 as follows:

28. (Twice Amended) A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing an inner dielectric element;

(b) providing first and second metal layers having openings therein on opposite surfaces of said inner dielectric element, said openings defining edges in said first and second metal layers, each said opening in said first metal layer being in substantial alignment with one of said openings in said second metal layer;

(c) coating said inner dielectric element and said first and second metal layers and said edges of said first and second metal layers with a dielectric material to thereby form a coated structure having first and second outer dielectric layers covering the first and second metal layers respectively and having dielectric material in said openings of said first and second metal layers and covering said edges of said first and second metal layers;

(d) forming one or more through vias extending through said coated structure, each said through via being in substantial alignment with said aligned openings in said first and second metal layers;

(e) providing first and second outer metal layers covering said outer dielectric layers;

(f) metalizing said [coated] through vias to form metallic via liners connecting said outer metal layers, said dielectric material extending into [lining] said vias being disposed between the metallic via liners and said first and second metal layers [by dielectric material of said coated structure].

REMARKS

The present preliminary amendment is intended to address issues raised in the Official Action mailed October 25, 1999 in the parent case. In regards to applicant's amendment, claim 28 has been amended to clarify that what is being claimed is the embodiment as shown in Figures 10 and 11. Claim 28 has been amended to clarify that the dielectric material does not cover the edges of the inner dielectric layer after the vias are formed. The Examiner's indication in the interview summary of May 22, 2000 that it appears that the proposed amendment to claim 28 would overcome the primary reference to *Gall et al.* is appreciated.

In the parent case, claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34 were rejected under 35 U.S.C. § 103 as being unpatentable over *Gall et al.* (U.S. Patent 5,659,951) in view of *DiStefano et al.* (U.S. Patent 5,282,312). This rejection should not be repeated in the present case. The Examiner in the Office Action dated October 25, 1999 indicated that the patent to *Gall et al.* discloses a method of making a multi-layer circuit assembly including: providing an inner dielectric element 30e; providing first and second metal layers 26b, 26c; coating the inner dielectric layer and first and second metal layers with first and second outer dielectric layers 30d, 30g; forming one through vias 65 through the coated structure; providing a first outer metal layer 24b over the first outer dielectric layer 30d and a second outer metal layer 24d under the second outer dielectric layer 30g; and metalizing the coated through vias to form liners 40. The Examiner acknowledged, however, that *Gall* does not disclose that the dielectric material is formed by coating to form a coated structure.

The Examiner in the parent case alleged that *DiStefano et al.* teaches disposing flowable dielectric material by coating to form sheetlike layers of material for electrical circuit assemblies. The Examiner has indicated that this teaching is disclosed in col. 7, lines 29-47 of *DiStefano et al.* The Examiner's motivation to combine the *Gall et al.* reference and *DiStefano et al.* references in the parent case was that one of ordinary skill in the art at the time the invention was made would have known to modify the invention disclosed by *Gall et al.* by coating the dielectric material and the dielectric element to form sheetlike laminated layers of material for electric circuit assemblies, as disclosed by *DiStefano et al.*

However, the Office Action in the parent case did not allege that *DiStefano et al.* teaches applicant's step of forming dielectric layers and a dielectric liner in the vias, as claim 1 now requires. In claim 1, the recited process includes coating the metal layers and the through vias with a dielectric, then providing outer metal layers over said first and second outer dielectric layers, and metalizing said coated through vias to form metallic via liners connecting said outer metal layers. The metal via liners are separated from the first and second metal layers by the dielectric. Thus, the via liners are insulated from the first and second metal layers, except where an external connection is provided. With respect to claim 28 and its dependent claims, neither *Gall et al.* nor *DiStefano et al.* disclose coating an inner dielectric element and first and second metal layers with a dielectric material to form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively, as claim 28 requires.

A review of *Gall et al.* and *DiStefano et al.* reveals that they do not disclose all the limitations set forth in claims 1 and 28. As noted above, the Examiner in the parent case relied upon col. 7, lines 29-47 of *DiStefano et al.* in his rejection of claims 1 and 28. As shown in FIG. 5 for example, *DiStefano et al.* discloses a method of making multi-layer circuit assemblies utilizing a plurality of circuit panels 10 and interposers 12. Each interposer is disposed between two circuit panels. Each interposer has a flowable dielectric material on its major surfaces except at its interconnect locations. During the lamination process, some of the flowable dielectric material is forced into the vias. While the cited passage of *DiStefano et al.* discloses that dielectric material collects in reservoirs formed in via holes, *DiStefano et al.* does not disclose that the dielectric material lines the via holes, nor does it suggest subsequently depositing a metal layer in the through vias over the dielectric liner, as claim 1 requires. The art cited by the Examiner does not suggest that one would deposit a metal layer on any such dielectric material. Indeed, because the dielectric material referred to in this passage of the reference only enters the <u>inside</u> of the via liners <u>during</u> the lamination process, it is not seen how one could metalize the through via after that dielectric material is forced into the interior of the via liners. Further, the dielectric layer formed between the circuit panels and the interposer does not coat an inner dielectric element, as claim 28 requires. Accordingly, the combination of the *Gall et al.* reference and *DiStefano et al.* cannot render any of the previously rejected claims obvious.

Accordingly, since *Gall et al.* and *DiStefano et al.* do not render claims 1 or 28 obvious, they do no make any of the

claims that depend upon claims 1 and 28 obvious. For the reasons set forth above, the 103 rejection should not be repeated with respect to claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34.

The Examiner next rejected claims 6 and 31 in the parent case under 35 U.S.C. § 103(a) as being unpatentable over *Gall et al.* in view of *DiStefano et al.*, as applied to claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34 and further in view of *Tamm et al.* (U.S. Patent 5,666,722). As noted above, neither *Gall et al.* nor *DiStefano et al.* combined teach all of the limitations of the claims recited above. The Examiner applied the *Tamm et al.* reference in the parent case to teach metalizing the blind vias and through vias simultaneously. However, *Tamm et al.* also has not been asserted as teaching the limitations missing from *Gall et al.* in view of *DiStefano et al.* as previously discussed. Accordingly, the combination of the inventions disclosed by *Gall et al.*, *DiStefano et al.* and *Tamm et al.* does not render any of applicant's claims obvious.

The Examiner next rejected claim 11 in the parent case under 35 U.S.C. § 103(a) as being unpatentable over *Gall et al.* in view of *DiStefano et al.* as applied to claims 1-5, 7-10, 12-14, 15, 17, 19-25, 28-30 and 32-34 above, and further in view of *Brauer et al.* (U.S. Patent 5,153,986). As previously stated, the combination of *Gall et al.* and *DiStefano et al.* does not teach all of applicant's claimed limitations as set out in claims 1 and 28. The Examiner has previously applied the *Brauer et al.* reference to teach depositing a seed layer over the first outer dielectric layer and under the second dielectric layer including the first and second metal layers.

However, the *Brauer et al.* patent has not been asserted as teaching the limitations missing from the *Gall et al.* reference. Accordingly, the combination of the inventions disclosed by *Gall et al.*, *DiStefano et al.* and *Brauer et al.* cannot render any of applicant's claims obvious.

The Examiner next rejected claims 16, 18, 26 and 27 in the parent case under 35 U.S.C. § 103(a) as being unpatentable over *Gall et al.* The Examiner indicated that it would have been an obvious design choice to choose any desired dimension of thickness for the dielectric material, diameter of through vias and first and second metal layers since applicant has not disclosed that the claimed dimension of thickness solves any stated problem. It is applicant's assumption that since claim 1 was rejected under *Gall et al.* in view of *DiStefano et al.*, it was the Examiner's intention to reject claims 16, 18, 26 and 27 under *Gall et al.* in view of *DiStefano et al.* Again, since *Gall et al.* and *DiStefano et al.* fail to disclose all of applicant's claimed limitations in claims 1 and 28, the combination of *Gall et al.* and *DiStefano et al.* cannot make obvious any of applicant's dependent claims. Also, it is not clear on this accord as to whether *Gall et al.'s* drilling process would be practiced with a 200 micron (.0078") diameter hole, to yield an insulated hole of 150 microns (.006"), as recited in claim 18, one would need a .006 inch drill and the ability to place such a drill and keep it on a straight path through the multiple layers.

As it is believed that all rejections and requirements set forth in the Official Action dated October 25, 1999 in the parent case have been fully met by the foregoing preliminary amendment and remarks, favorable reconsideration and allowance of the application are earnestly solicited.

If there are any additional charges in connection with this Preliminary Amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor. If the Examiner has any questions, we respectfully ask that the Examiner contact the undersigned at the address, telephone and facsimile information set forth below.

Respectfully submitted,

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METHOD FOR FORMING A MULTI-LAYER CIRCUIT ASSEMBLY

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of United States Provisional Patent Application Serial No. 60/032,967 filed December 13, 1996, the disclosure of which is incorporated by reference herein.

FIELD OF THE INVENTION

The present invention relates to the field of electrical circuitry, and more particularly relates to the fabrication of individual panels with multiple layers.

BACKGROUND OF THE INVENTION

There continues to be an ever increasing need for multi-layer electronic assemblies which provide high density, complex interconnections for electrical components. Methods for forming multi-layer electronic assemblies are taught in Dux et al., U.S. Patent 5,224,265 and Ehrenberg et al. U.S. Patent 5,232,548. The '265 patent discloses a high-density, multi-layer thin film structure and process for making a multi-layer structure wherein multiple individually testable sub-units are fabricated in parallel, pre-tested for operational performance, and joined together to form a three dimensional wiring matrix.

Commonly assigned U.S. Patent No. 5,590,460 to DiStefano et al., the disclosure of which is incorporated by reference herein, teaches a process for making a multi-layered assembly including providing a sheet of a dielectric material having a top and a bottom surface. Layers of a temporary layer susceptible to etching are coated on the top and bottom surfaces of the dielectric sheet, respectively. Photoresist layers are then applied over the top and bottom temporary layers and are photographically exposed to develop openings which are perpendicular to the external

surfaces of the assembly. The assembly is then exposed to an etchant to form aligned apertures in the top and bottom temporary layers. After formation of the holes, an electrically conductive structural material such as a metal is deposited within each hole and within the apertures in the top and bottom temporary layers. A structural material is then applied as a continuous layer covering the peripheral surfaces of the holes in the sheet and also covering the peripheral walls of the apertures in the temporary layers.

Despite these and other efforts in the art, there are needs for still further improvement.

SUMMARY OF THE INVENTION

According to one embodiment of the invention, a method of making a multi-layer circuit assembly includes providing a core structure having an inner dielectric element with first and second metal layers on opposite surfaces thereof. The dielectric element, such as a polyimide material, is preferably between about 25 to 50 microns thick. The first and second metal layers may comprise a highly conductive material such as copper and each metal layer is generally about are 1 to 18 microns thick. In one embodiment, the first metal layer on top of the dielectric element could serve as a ground plane and the second metal layer on the bottom surface of the dielectric element could serve as a power plane. The first and second metal layers will also act as a backbone for the final assembly to provide rigidity thereto. The specific composition of the first and second metal layers may vary depending upon the specific application for which the final assembly will be used, which in turn will determine the thermal coefficient of expansion and the ultimate dimensional stability of the assembly.

In the next stage of the process, one or more through vias are formed through the metal layers and the inner dielectric element. The through vias may be created by a variety of well know techniques such as

punching, laser drilling or plasma etching. The through vias should extend entirely through the first metal layer, the dielectric element and the second metal layer. The exact location of the through vias may vary depending upon the specific requirements of the final assembly. In one preferred embodiment, the through vias may be formed by first etching the metal layers to form aligned holes therein, aligning a laser with the aligned holes and laser drilling through the dielectric element. In another embodiment, a YAG laser may be used. In a first drilling step, the first and second metal layers are drilled while the YAG laser is on high power. In a second drilling step, the dielectric element is drilled while the YAG laser is on low power. As will be discussed in more detail below, although laser drilling may be slightly more costly than plasma etching, laser drilling provides for better alignment of the holes in the metal layers with the holes in the dielectric element. In addition, the side walls formed using a laser are more uniform than those formed with etching techniques.

After the through vias have been formed, the first and second metal layers and the through vias are coated with a dielectric material, such as a polyimide or an epoxy, to form a coated structure having first and second outer dielectric layers. The dielectric material is applied using well known techniques such as dipping, spin coating and plating techniques (e.g. preferably electrophoretic plating). During the coating process, all of the exposed surfaces of the metal layers, including the side walls of the through vias, are covered by the dielectric material. The thickness of the dielectric material coating should be uniform. For example, in certain preferred embodiments, after the coating step, the outer dielectric layers have a uniform thickness of approximately 25 to 75 microns. The exact thickness of the dielectric material is controlled so that the through vias remain open after the coating process. For example, in certain embodiments, the diameter of the through vias is approximately 175 to 200 microns before the

coating process and approximately 25 to 150 microns after the coating process.

In the next stage of the process, outer metal layers comprising highly conductive materials such as copper are provided over the first and second outer dielectric layers, respectively. The step of providing the outer metal layers over the first and second outer dielectric layers may include the steps of seeding the exterior surface of the outer dielectric layers, such as by exposure to a liquid seeding process or by sputter deposition. For example, an adhesion promoting layer of a conductive base, such as a graphite seed, may be applied. The seed layer contacts the first and second outer dielectric layers. The outer metal layers are then electroplated over the seed layer as by connecting an electroplating potential source to the first and the second metal layers and immersing the assembly in an electroplating bath with a counter electrode. The outer metal layers may also be provided using electroless plating or sputtering techniques. The outer metal layers substantially conform to the shape of the first and second outer dielectric layers. Each outer metal layer preferably has a thickness of approximately 1 to 18 microns and most preferably a thickness of approximately 1 to 6 microns; however, the exact thickness of the outer metal layers will depend upon the particular application for which the assembly will be used. Finally, the coated through vias are metallized to form metallic via liners which are connected to the outer metal layers and which are insulated from the first and second metal layers.

In other preferred embodiments, the adhesion between the outer metal layers and the first and second outer dielectric layers may be enhanced by providing a tie coat including nickel and chrome. In these embodiments, the nickel/chrome tie coat is provided directly over the outer dielectric layers and then a seed layer, such as copper, is provided over the

tie coat. Finally, another layer of copper, which is thicker than the seed layer, is provided over the seed layer.

In the next stage of the process signal lines are formed by selectively patterning the outer metal layers to form first signal lines overlying the first metal layer and second signal lines overlying the second metal layer. The selectively patterning step includes the step of selectively removing portions of the outer metal layers such as by selectively etching the outer metal layers. In one embodiment, a photo-resist layer is provided over the outer metal layers and the layers are then subjected to an etching process to pattern the signal lines therein. In other embodiments the selectively patterning step may include the step of selectively depositing the outer metal layers. The first signal lines are substantially parallel to one another and substantially perpendicular to the second signal lines. In turn, the second signal lines are substantially parallel to one another. After the signal lines have been formed, the assembly may be used to electrically connect circuit elements on the same side of the assembly or on opposite sides thereof. The above-described methods provide economical processes of making a multi-layer circuit assembly. The same techniques may be used with a different number of layers to provide a circuit assembly having numerous layers whereby several of the structures described above can be laminated together. For example, the lamination techniques disclosed in U.S. Patent No. 5,282,312, the disclosure of which is incorporated herein by reference, may be employed.

In other embodiments, blind via openings may be formed through the outer dielectric layers to expose one or more regions of the first and second metal layers. The blind vias may be formed by placing a mask over the first and second outer dielectric layers and scanning a laser over the mask so that laser light passes through apertures in the mask to cut through the dielectric material. During the laser drilling step, substantially all of the

dielectric material is removed from the blind vias; however, a slight residue of dielectric material may remain at the closed ends of one or more of the blind vias adjacent the exposed regions of the first and second metal layers. The residue in the blind vias, which typically has a thickness of less than one micron, may be removed by subjecting the assembly to a plasma etching process. Although it is preferable to remove the residue using a plasma etching process so that all of the blind vias may be simultaneously treated, it is also possible to use a YAG laser to remove the residue. However, the use of a laser to remove the residue may prove time consuming because typically the laser must be aligned with each of the blind via openings. After the blind vias have been formed, one or more regions of the first and second metal layers are exposed and accessible through the blind vias. The blind vias are then metallized so that at least some of the signal lines are connected to the first and second metal layers. The steps of metallizing the through vias and metallizing the blind vias may be performed simultaneously.

In another embodiment of a method of making a multi-layer circuit assembly, the method includes providing an inner dielectric element and first and second metal layers having openings therein on opposite surfaces of the inner dielectric element, whereby each opening in the first metal layer is in substantial alignment with one of the openings in the second metal layer. For example, first and second metal layers having a plurality of apertures therein may be provided and the metal layers may be laminated to opposite surfaces of a dielectric element so that the openings in the first and second metal layers are in substantial alignment. Lamination techniques are disclosed in commonly assigned U.S. Patent No. 5,583,321, the disclosure of which is incorporated herein by reference The inner dielectric element and the first and second metal layers are then coated with a dielectric material, using the coating processes described above, to thereby

form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively. Next, through vias are formed through the coated structure, whereby each through via is in substantial alignment with the aligned openings in the first and second metal layers. For example, a laser may be aligned with the aligned openings in the metal layers for simultaneously drilling through the outer metal layers and the dielectric element to provide one or more through vias. During the drilling step, it is critical that the diameter of the laser cut be controlled so that the first and second metal layers remain covered by the dielectric material and are not exposed at the side walls of the through vias. In alternative embodiments, the through vias may be formed using the etching or punching techniques described above. After the through vias have been formed, a final multi-layer assembly may be fabricated using the processes described above.

In another embodiment of the present invention, the first and second outer metal layers may be provided over the outer dielectric layers before the blind vias are formed in the outer dielectric layers. The outer metal layers according to this embodiment may be laminated to the outer dielectric layers or may be applied using a plating technique or sputtering technique. The blind vias may then be formed through the outer metal layers and the outer dielectric layers using the various techniques described above in order to expose one or more regions of the first and second metal layers. Next, the blind vias may be metallized so that at least some of the signal lines are connected to the first and second metal layers. The metal in the blind vias may be provided using electroless plating and sputtering techniques.

In other embodiments, additional signal lines may be formed in at least one of the first and second metal layers before the coating step. For example, signal paths for carrying critical signals may be etched into the

first and second metal layers, and the signal paths insulated during the coating with a dielectric material step.

These and other objects, features and advantages of the present invention will be more readily apparent from the detailed description of the preferred embodiments set forth below, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1. is a fragmentary diagrammatic sectional view depicting portions of a multi-layer circuit assembly during one step of a fabrication process according to one embodiment of the invention.

Figs. 2-8 are views similar to Fig. 1 but depicting the multi-layer circuit assembly during later stages of the same process.

Fig. 9 is a perspective view of one embodiment of a multi-layer circuit element manufactured in accordance with the assembly steps shown in Figs. 1-8.

Fig. 10 is a fragmentary diagrammatic sectional view depicting portions of a multi-layer circuit assembly during one step of a fabrication process according to another embodiment of the invention.

Fig. 11 is a view similar to Fig. 10 but depicting the multi-layer circuit assembly during later stages of the same process.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A method in accordance with one embodiment of the present invention begins with a core structure 20 including an inner dielectric element 22 having a first or top surface 24 and a second or bottom surface 26. The inner dielectric element 22 includes a material having a relatively high elastic modulus such as a polyimide material. One suitable polyimide material is available under the trade name UPILEX from the Ube Corporation. The dielectric element may also include an epoxy or a FR4

circuit board. The dielectric element is preferably about 25 to 50 microns thick.

A first metal layer 28 is provided over the first surface 24 of the inner dielectric element 22 and a second metal layer 30 is provided over the second or bottom surface 26 of the dielectric element 22. The first and second metal layers 28 and 30 may be assembled with the inner dielectric element 22 using the lamination techniques disclosed in commonly assigned U.S. Patent Application Serial No. 5,583,321, the disclosure of which is incorporated herein by reference. The first and second metal layers 28, 30 preferable comprise materials having highly conductive properties such as copper, gold and bronze or alloys or composites thereof; however, the exact composition of the metal layers 28, 30 may vary based upon the particular application for which the multi-layer circuit assembly will be utilized. The composition of the first and second metal layers 28, 30 will determine the coefficient of thermal expansion and the overall dimensions of the final assembly. Preferably the first and second metal layers 28, 30 are each between approximately 1 to 18 microns thick. In addition, the first and second metal layers will provide rigidity for the final assembly.

In the next stage of the process, one or more via holes are formed through the first and second metal layers 28, 30 and the inner dielectric element 22 and are hereinafter referred to as "through vias." The exact location of the through vias will depend upon the particular application for which the final circuit assembly is to be utilized. Referring to Fig. 2, during an initial stage of forming the through vias, a plurality of holes are created in the first and second metal layers 28, 30 by well known techniques, such as etching. In other embodiments, the holes in the first and second metal layers 28, 30 are created by techniques such as photo processing, plasma etching, punching and laser drilling. Each hole 32 in the first metal layer 28 is in substantial alignment with one of the holes 34 in the

second metal layer 30. After the holes 32 and 34 have been formed, the metal layers 28, 30 serve as a mask and an opening in alignment with the holes 32, 34 is drilled through the inner dielectric element 22 using a laser, such as a CO_2 laser.

Fig. 3 shows the core structure 20 after one or more through vias 36 have been formed therein. Each through via 36 extends entirely through the metal layers 28, 30 and the inner dielectric element 22, i.e. from the exterior surface 38 of the first metal layer 28 to the exterior surface 40 of the second metal layer 30. The through vias 36 extend in a direction which is substantially perpendicular to horizontal planes (not shown) formed by the first and second surfaces 24, 26 of the dielectric element 22. Each through via 36 includes one or more side walls 42 which define the diameter of the via 36. The above-described process for forming the through vias 36 comprises at least two steps including etching the first and second metal layers 28, 30 and laser drilling the inner dielectric element 22. However, other methods may be used, such as simultaneously punching through the first and second metal layers 28, 30 and the dielectric element 22, or using a YAG laser to drill through the metal layers 28, 30 at high power and through the inner dielectric element 22 while the YAG laser is at low power. Although using a laser to form through vias may prove more costly than certain etching techniques, there are advantages to using a laser drill, such as more accurate alignment of the through vias 36 and formation of uniform side walls 42. In contrast, chemical etching techniques are not effective for controlling the uniformity and configuration of the through via side walls, e.g. the side walls are generally irregular in shape, sloped and/or curved.

Referring to Fig. 4, in the next stage of the process, the metal layers 28, 30, and the through vias 36 are coated with a dielectric material to form an at least somewhat conformally coated structure having first and

second outer dielectric layers 47, 49 which overlie the first and second metal layers 28, 30, respectively. Various techniques may be used for coating the metal layers 28, 30 and the through vias 36 including dipping the structure in a dielectric material solution, spin coating or plating (e.g., as electrophoretic plating). After the coating step, the outer dielectric layers 47, 49 should have a uniform thickness and should not have any voids or pin-holes therein. The outer dielectric layers 47, 49 may be one of any number of different materials such as a photosensitive or a non-sensitive polyimide, epoxy or other dielectric material. As mentioned above, during the coating step the dielectric material also lines the side walls 42 of the through vias. The specific thickness of the dielectric material is controlled so that the through vias 36 remain open and are not clogged after the coating step. For example, before the coating step each through via 36 is preferably between 150 to 250 microns in diameter and after the coating step each through via 36 is preferably between 50 and 150 microns in diameter. When using the electrophoretic plating technique, the amount of dielectric material applied may be controlled by regulating the voltage level and the specific composition of the electrophoretic material.

Referring to Fig. 5, in the next stage of the process, blind vias are formed through the outer dielectric layers 47 and 49 to expose one or more regions of the first and second metal layers 28, 30. A first set of blind vias 46 are formed through the first outer dielectric layer 47 to expose portions of the first metal layer 28 and a second set of blind vias 48 are formed through the second outer dielectric layer 49 to expose portions of the second metal layer 30. The blind vias 46, 48 are formed by placing a mask (not shown) over the first and second outer dielectric layers 47, 49 and scanning the dielectric material with a laser. During the scanning step, the laser will pass through openings in the mask to form the blind via openings 46, 48. A slight residue of dielectric material, having a thickness of

generally less than about 1 micron, may remain in the closed ends of the blind vias 46, 48. The residue is preferably removed by using a plasma etching technique which simultaneously removes the residue from all of the blind vias 46, 48; however, the residue may also be removed using a laser drilling technique.

Referring to Fig. 6, in the next stage of the process, the first and second outer dielectric layers 47 and 49, the through vias 36 and the blind vias 46, 48, including the exposed regions of the first and second metal layers 28, 30 accessible through the closed ends of the blind vias 46, 48, are seeded with a conductive material 50 to provide a base for the formation of thicker outer metal layers thereover. Although the present invention is not limited by any particular theory, it is generally believed that a metal layer may not be reliably applied directly to dielectric material and therefore, the dielectric material is primed for receiving the outer metal layers by seeding the dielectric material with a conductive seed layer 50. The seed layer 50 typically comprises materials such as graphite. In other embodiments, the seeding technique may also include sputtering or electroless plating processes.

Referring to Fig. 7, outer metal layers 52, such as copper, are then deposited as a continuous layer over the conductive seed layer 50 and within the through vias 36 and the blind vias 46, 48 by using plating techniques. The plating technique may include electroless plating, electroplating or sputtering. Metals selected from the group consisting of gold, copper, tin, nickel and alloys or combinations thereof are preferred. Copper is particularly preferred where the outer metal layers 52 include only one metal. The outer metal layers 52 are preferably about 1 to 18 microns thick and most preferably between about 1 to about 6 microns thick.

Referring to Figs. 8 and 9, the assembly may then be circuitized by selectively patterning the outer metal layers to form first signal lines 54 overlying the first metal layer 28 and second signal lines 56 overlying the second metal layer 30. The signal lines may be formed by using standard photoresist and etching techniques. In one embodiment, the first signal lines 54 are substantially parallel to one another and run in the direction generally designated "X" while the second signal lines 56 are also substantially parallel to one another and run in the direction generally designated "Y". The first signal lines 54 and the second signal lines 56 are substantially perpendicular to one another. In other embodiments, the step of selectively patterning the outer metal layers includes selectively depositing the outer metal layers over the outer dielectric layers.

Referring to Figs. 10 and 11, in a method of forming a multi-layer assembly according to another embodiment, an inner dielectric element 122, substantially similar to that described above, is provided and first and second metal layers 128, 130 having openings therein are laminated to opposite sides of the dielectric element 122. The openings 132, 134 in the first and second metal layers 128, 130 are aligned so that each pair of openings 132, 134 are in substantial alignment. Next, the inner dielectric element and the first and second metal layers 128, 130 are coated with a dielectric material 144, according to processes as described above. Through vias (defined by imaginary lines 142) are then formed through the coated structure using the techniques described above to provide a partially finished assembly substantially similar to that shown in Fig. 4. The assembly is then completed using processes similar to those described above and shown in Figs. 5-8.

Numerous variations and combinations of the features described above can be utilized without departing from the present invention as defined by the claims. In one such variant, the core structure may be

assembled by laminating sheet metal to the exposed surfaces of the inner dielectric element. In other embodiments, the outer metal layers may be provided by laminating sheet metal over the outer dielectric layers after the coating step. In the latter embodiment, after the outer metal layer has been formed over the outer dielectric layers, the outer metal layer is subjected to a laser drilling process to form the blind vias and the assembly is then subjected to a plating process to provide a second outer metal layer in the blind vias and over the exposed regions of the first and second metal layers accessible through the blind vias.

In other embodiments, additional signal lines may be formed on the first and second metal layers. The additional signal lines may be etched into either of the first or second metal layers and then insulated with a dielectric material. The additional signal lines may be used for critical signal paths so the signals can be routed through the assembly using the shortest possible path and to avoid interference from other signal lines. Typically, in the final assembly, the first metal layer will act as a ground plane and the second metal layer will act as a power plane. However, in other preferred embodiments the first metal layer may be the ground plane and the second metal layer may be the power plane. Alternatively, both metal layers may be power planes or both may be ground planes. Further, either the first or second metal layers may act as both a power plane and a ground plane.

Although the foregoing techniques provide economical methods of making a multi-layer circuit assembly which has four layers, the same processes may be used to form assemblies having a different number of layers. For example, to provide a circuit assembly with numerous layers, several of the assemblies described above can be laminated together using such lamination techniques as disclosed in commonly assigned U.S. Patent No. 5,282,312, the disclosure of which is incorporated herein by reference.

As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration, rather than by way of limitation of the invention described in the claims.

We Claim:

1. A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing a core structure including an inner dielectric element having first and second metal layers on opposite surfaces thereof;

(b) forming one or more through vias extending through said metal layers and said inner dielectric element;

(c) coating said metal layers and said through vias with a dielectric material to thereby form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively and dielectric material lining said through vias;

(d) providing outer metal layers over said first and second outer dielectric layers ;

(e) metallizing said coated through vias to form metallic via liners connecting said outer metal layers and insulated from said first and second metal layers.

2. A method as claimed in claim 1 further comprising the step of selectively patterning said outer metal layers to form first signal lines overlying said first metal layer and second signal lines overlying said second metal layer.

3. A method as claimed in claim 1, wherein said first metal layer includes a ground plane and said second metal layer includes a power plane.

4. A method as claimed in claim 1, wherein said first signal lines are substantially perpendicular to said second signal lines.

5. A method as claimed in claim 1 further comprising the steps of forming blind vias through said outer dielectric layers to expose one or more regions of said first and second metal layers and metallizing said blind vias so that at least some of said signal lines are connected to said first and second metal layers.

6. A method as claimed in claim 5 wherein said steps of metallizing said blind vias and metallizing said through vias are performed simultaneously.

7. A method as claimed in claim 2, further comprising the step of forming additional signal lines in at least one of said first and second metal layers before the coating step.

8. A method as claimed in claim 1, wherein each said through via has side walls, said side walls being covered by said dielectric material during the coating step.

9. A method as claimed in claim 1, wherein the selectively patterning step includes the step of selectively removing portions of the outer metal layers.

10. A method as claimed in claim 9 wherein the selectively patterning step includes the step of selectively etching the outer metal layers to form said first and second signal lines therein.

11. A method as claimed in claim 5, wherein the step of providing outer metal layers over the first and second outer dielectric layers includes the step of:

depositing a seed layer over said outer dielectric layers including the blind vias and the exposed regions of said first and second metal layers;

plating or sputtering a metal onto said seed layer.

12. A method as claimed in claim 2 wherein said step of selectively patterning said outer metal layers includes the step of selectively depositing said outer metal layers.

13. A method as claimed in claim 5, wherein the step of forming said blind vias includes the step of laser drilling said outer dielectric layers.

14. A method as claimed in claim 13, further comprising the step of plasma etching said blind vias after the laser drilling step to remove any said dielectric material residue remaining in said blind vias.

15. A method as claimed in claim 1, wherein during the coating step said dielectric material is provided having a uniform thickness.

16. A method as claimed in claim 1, wherein after the coating step said dielectric material has a uniform thickness of approximately 25-75 microns.

17. A method as claimed in claim 1, wherein after the coating step said through vias remain open.

18. A method as claimed in claim 1, wherein said through vias have a diameter of approximately 175-200 microns before the coating step and approximately 25-150 microns after the coating step.

19. A method as claimed in claim 1, wherein the coating step includes the step of electrophoretically depositing said dielectric material.

20. A method as claimed in claim 1, wherein the coating step includes the step of dipping said core structure in said dielectric material.

21. A method as claimed in claim 1, wherein the coating step includes the step of spin coating said core structure with said dielectric material.

22. A method as claimed in claim 1, wherein the step of forming said through vias includes the steps of etching said first and second metal layers and drilling said inner dielectric element.

23. A method as claimed in claim 1, wherein the step of forming said through vias includes punching said first and second metal layers and said inner dielectric element.

24. A method as claimed in claim 1, wherein the step of forming said through vias includes the step of plasma etching.

25. A method as claimed in claim 1, wherein the step of forming said through vias includes the steps of:

etching said first and second metal layers to provide aligned openings therein;

aligning a laser in one of said aligned openings and drilling said inner dielectric element.

26. A method as claimed in claim 1, wherein said first and second metal layers are approximately 1-18 microns thick.

27. A method as claimed in claim 1, wherein said inner dielectric element is approximately 25-50 microns thick.

28. A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing an inner dielectric element;

(b) providing first and second metal layers having openings therein on opposite surfaces of said inner dielectric element, each said opening in said first metal layer being in substantial alignment with one of said openings in said second metal layer;

(c) coating said inner dielectric element and said first and second metal layers with a dielectric material to thereby form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively;

(d) forming one or more through vias extending through said coated structure , each said through via being in substantial alignment with said aligned openings in said first and second metal layers;

(e) providing first and second outer metal layers over said outer dielectric layers;

(f) metallizing said coated through vias to form metallic via liners connecting said outer metal layers and insulated from said first and second metal layers by dielectric material of said coated structure;

29. A method as claimed in claim 28 further comprising the step of selectively patterning said outer metal layers to form first signal lines

overlying said first metal layer and second signal lines overlying said second metal layer.

30. A method as claimed in claim 28 further comprising the steps of forming blind vias through said outer dielectric layers to expose one or more regions of said first and second metal layers and metallizing said blind vias so that at least some of said signal lines are connected to some first and second metal layers.

31. A method as claimed in claim 30, wherein the steps of metallizing said through vias and metallizing said blind vias are performed simultaneously.

32. A method as claimed in claim 28, wherein said first metal layer includes a ground plane and said second metal layer includes a power plane.

33. A method as claimed in claim 29, wherein said first signal lines are substantially perpendicular to said second signal lines.

34. A method as claimed in claim 33, wherein the selectively patterning step includes the step etching the outer metal layers.

ABSTRACT OF THE DISCLOSURE

A method of making a multi-layer circuit assembly includes providing a core structure including an inner dielectric element having first and second metal layers on opposite surfaces thereof, forming one or more through vias extending through the metal layers and the inner dielectric element and coating the metal layers and the through vias with a dielectric material to form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively and dielectric material lining the through vias. An outer metal layer is then provided over the first and second outer dielectric layers. The coated through vias are then metallized to form metallic via lines which connect the outer metal layers and which are insulated from the first and second metal layers. The outer metal layers are then selectively patterned to form first signal lines overlying the first metal layer and second signal lines overlying the second metal layer. In certain embodiments, blind vias may be formed through the outer dielectric layers to expose one or more regions of the first and second metal layers. The blind vias are then metallized so that at least some of the signal lines are connected to the first and second metal layers.

FIG. 1

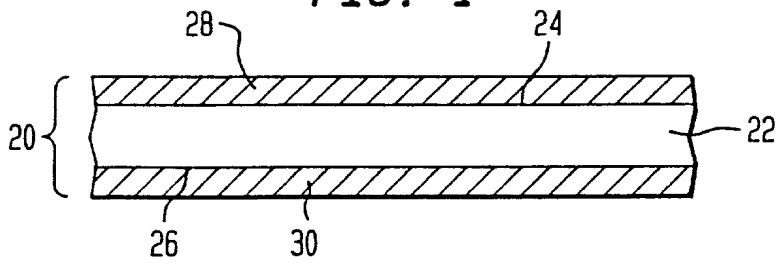


FIG. 2

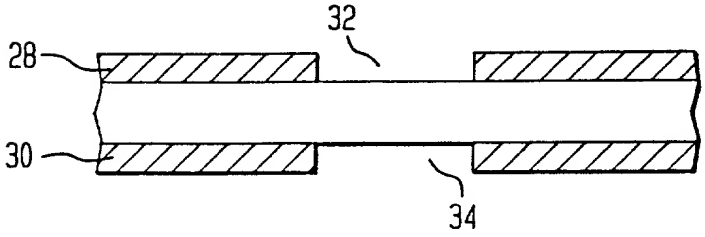


FIG. 3

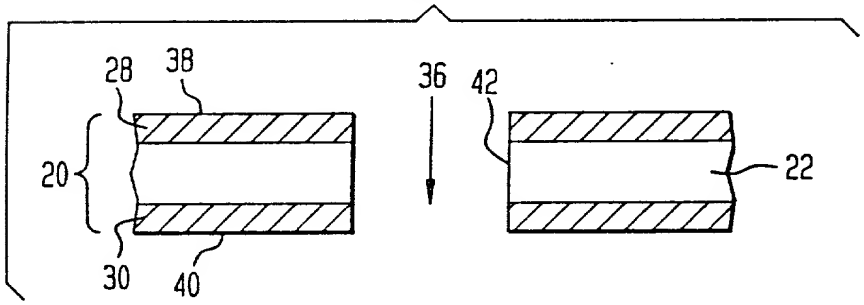


FIG. 4

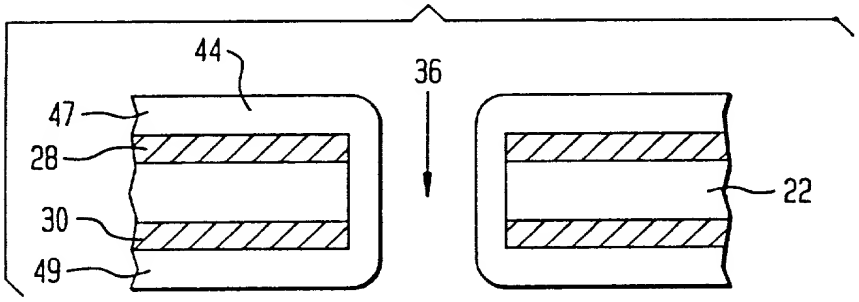


FIG. 5

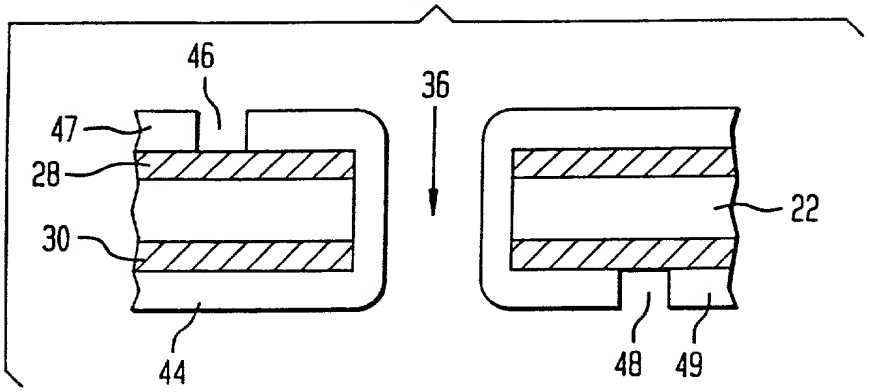


FIG. 6

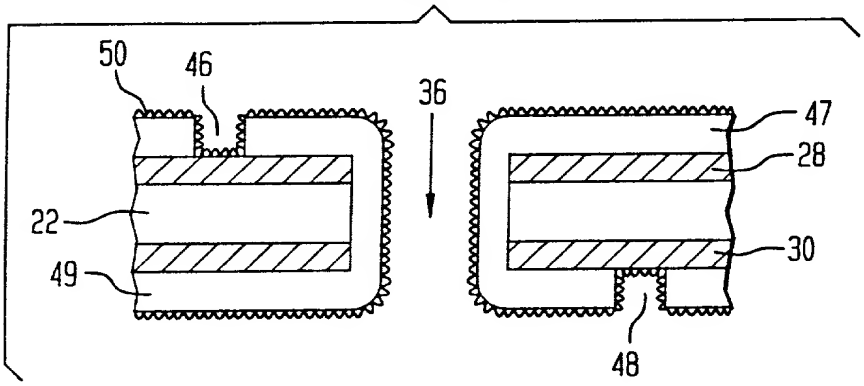


FIG. 7

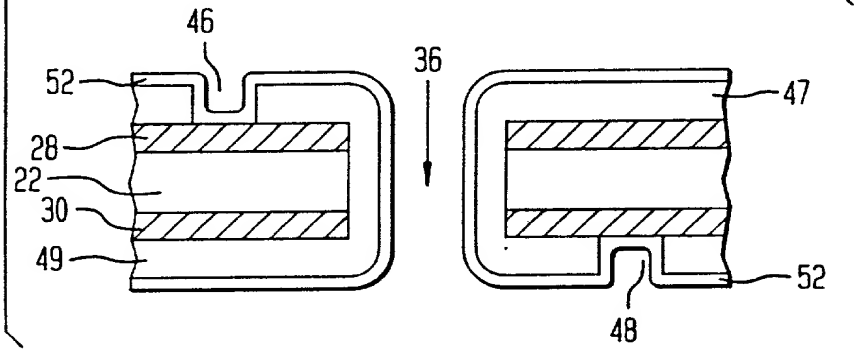


FIG. 8

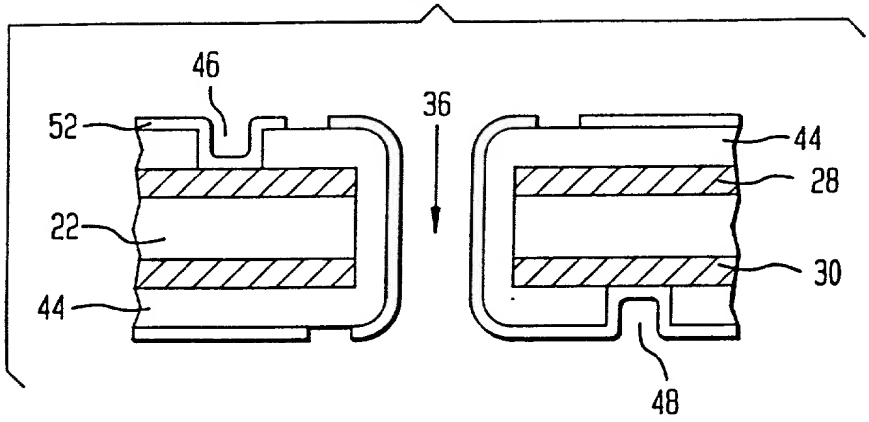


FIG. 9

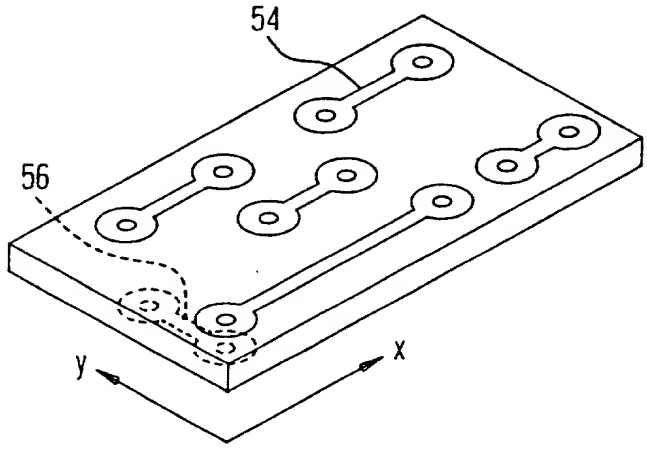


FIG. 10

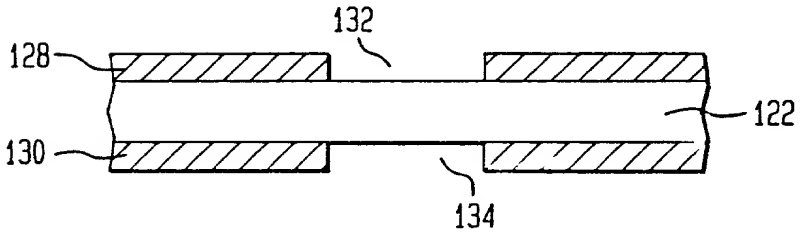
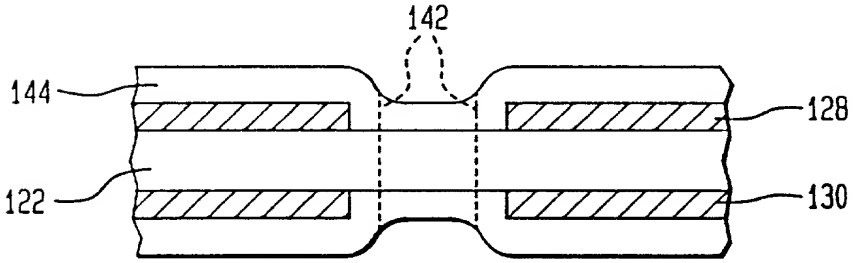


FIG. 11



DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

ATTORNEY'S DOCKET NO.: TESSERA 3.0-113

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR FORMING A MULTI-LAYER CIRCUIT ASSEMBLY the specification of which

☒ is attached hereto
☐ was filed on _____ as United States Application Number or PCT International Application Number_____and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (month, day, year)	PRIORITY CLAIMED
			YES ☐ NO ☐
			YES ☐ NO ☐
			YES ☐ NO ☐
LISTING OF FOREIGN APPLICATIONS CONTINUED ON PAGE 3 HEREOF ☐ YES ☒ NO			

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Application Number: 60/032,967 Filing Date: December 13, 1996

Application Number: Filing Date:

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Parent Application Serial Number: Parent Filing Date: Parent Patent No.:

U.S. Parent Application Serial Number: Parent Filing Date: Parent Patent No.:

PCT Parent Number: Parent Filing Date:

LISTING OF US APPLICATIONS CONTINUED ON PAGE 3 HEREOF: ☐ YES ☒ NO

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK 600 South Avenue West Westfield, New Jersey 07090	*(name and telephone number)* MICHAEL J. DOHERTY (908) 654-5000 Fax: (908) 654-7866

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature _____ **Date** 97.12.08

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Full name of second joint inventor, if any (given name, family name)

Second Inventor's signature _____ **Date** _____

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Post Office Address:

Full name of third joint inventor, if any (given name, family name):

Third Inventor's signature _____ **Date** _____

Residence: Citizenship:

Post Office Address:

Full name of fourth joint inventor, if any (given name, family name):

Fourth Inventor's signature _____ **Date** _____

Residence: Citizenship:

Post Office Address:

Full name of fifth joint inventor (given name, family name):

Fifth Inventor's signature _____ **Date** _____

Residence: Citizenship:

Post Office Address:

Full name of sixth joint inventor, if any (given name, family name):

Sixth Inventor's signature _____ **Date** _____

Residence: Citizenship:

Post Office Address:

Full name of seventh joint inventor, if any (given name, family name):

Seventh Inventor's signature _____ **Date** _____

Residence: Citizenship:

Post Office Address:

Full name of eighth joint inventor, if any (given name, family name):

Eighth Inventor's signature _____ **Date** _____

Residence: Citizenship:

Post Office Address:

☐ Additional inventors are being named on separately numbered sheets attached hereto.